Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.069”**

**N. WDO**

**RESET**

**N. MR**

**VCC**

**PFI**

**N. PFO**

**GND**

**N. RESET (RESET)**

**N. WDI/N.C.**

**PW27Y-6 Z**

**MASK**

**REF**

**.050”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035” min.**

**Backside Potential:**

**Mask Ref: PW27Y-6 Z**

**APPROVED BY: DK DIE SIZE .050” X .069” DATE: 4/18/16**

**MFG: MAXIM THICKNESS .010” P/N: MAX705**

**DG 10.1.2**

#### Rev B, 7/1